IN THE CLAIMS:

The claims are amended as follows:

1. (Currently Amended) ~~An integrated~~A circuit ~~with a~~for jitter measurement ~~circuit~~, comprising:

a plurality of delay elements~~, each delay element having an associated delay, an input configured to receive an input clock signal and an output responsive to the associated delay and the input clock signal, wherein the input clock signal has a significant instant;~~ arranged in a series-connected chain having a total delay equal to the sum of the delays of the delay elements, wherein the first element in the chain has an input that receives an input clock signal, the chain propagating the input clock signal through each of its elements, and each delay element output producing a delayed version of the signal on its input;

~~a first set of circuitry connected to the inputs and outputs of the plurality of delay elements, said first set of circuitry configured to detect the significant instant on the input clock signal, the first set of circuitry further configured to output a signal responsive to the significant instant on the input clock signal; and~~

a first set of circuitry operative to produce at an output a pulse corresponding to each delay element in response to the propagation of a significant instant of the input clock signal through the delay element, each pulse having a width that is approximately equal to the delay of the corresponding delay element; and

a second set of circuitry ~~configured to receive the signal responsive to the significant instant on the input clock signal and a first~~having one storage element corresponding to each output of the first set of circuitry, and an input that receives a trigger signal~~,~~ that is timed to correspond to a delay which is approximately half of the total delay of the chain, and

the second set of circuitry ~~further configured to latch onto the signal responsive to the significant instant on the input clock signal and further responsive to a significant instant on the first trigger signal, wherein a measure for jitter is determined from the latched signal responsive to the significant instant on the input clock signal.~~being operative to record in the corresponding storage element any pulse that is active at the time of occurrence of the trigger signal, wherein a jitter measurement is made based on the pulses recorded in the storage elements after a plurality of trigger signals has occurred.

2. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the output of one delay element is connected to the input of the next adjacent delay element~~associated delay of each delay element is approximately equal~~.

3. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the number of delay elements in the chain is N, where N is an even number greater than 2 and implemented as a power of 2~~the plurality of delay elements are serially connected together~~.

4. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the associated delay of each delay element is controlled by a delay control circuit.

5. (Currently Amended) The ~~integrated~~ circuit of claim 4, wherein at least one of the plurality of associated delays is not equal to any other of the plurality of associated delays, and wherein the delay control circuit is a charge pump controlled delay lock loop.

6. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the first set of circuitry includes a plurality of two-input logic gates~~,~~ with each of the plurality of two-input logic gates corresponding to ~~each~~ a respective one of the plurality of delay elements.

7. (Currently Amended) The ~~integrated~~ circuit of claim 6, wherein ~~the inputs~~ each of the plurality of two-input logic gates is coupled to the input and the output of a corresponding one of the plurality of delay elements.

8. (Currently Amended) The ~~integrated~~ circuit of claim 7, wherein one of ~~the~~ the two inputs of each ~~of the plurality of~~ two-input logic ~~gates~~gate is coupled to the output of its corresponding delay element ~~by means of~~via an inverter logic gate.

9. (Currently Amended) The ~~integrated~~ circuit of claim 7, wherein one of the two inputs of each of ~~the plurality of~~ two-input logic gates is coupled to the output of its corresponding delay element by means of wired connection.

10. (Currently Amended) The ~~integrated~~ circuit of claim 6, wherein each of the plurality of two-input logic gates is capable of producing a pulse with a width approximately equal to the delay of its corresponding delay element~~signal responsive to the significant instant on the input clock signal~~.

11. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the second set of circuitry includes a first plurality of latching circuits each ~~, each of the first plurality of latching circuits~~ corresponding to ~~each~~ one of the plurality of delay elements.

12. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the input clock signal is related to a reference clock signal.

13. (Currently Amended) The ~~integrated~~ circuit of claim 12, wherein the trigger signal is delayed by a first predetermined delay from the reference clock signal.

14. Cancelled.

15. (Currently Amended) The ~~integrated~~ circuit of claim 13, wherein a measure ~~for~~ of jitter is determined by comparing ~~the~~ a latched ~~signal responsive to the significant instant on the input clock signal~~pulse to the first predetermined delay.

16. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the measure ~~for~~ of jitter is filtered.

17. (Currently Amended) The ~~integrated~~ circuit of claim ~~16~~1, wherein the second set of circuitry further includes a single one detector for filtering the measure of jitter ~~is filtered by means of a single one detector~~.

18. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein ~~the latched~~ pulses are ~~signal responsive to the significant instant on the input clock signal is~~ recorded for a first number of significant instants ~~on~~ of the ~~first~~ trigger signal.

19. (Currently Amended) The ~~integrated~~ circuit of claim ~~1~~81, further comprising a third set of circuitry for recording pulses~~wherein the latched signal responsive to the significant instant on the input clock signal is recorded by a third set of circuitry~~.

20. (Currently Amended) The ~~integrated~~ circuit of claim 19, wherein the third set of circuitry includes a second plurality of latching circuits~~,~~ each ~~of the second plurality of latching circuits~~ corresponding to ~~each~~ one of the plurality of delay elements.

21. (Currently Amended) The ~~integrated~~ circuit of claim 20, wherein each of the second plurality of latching circuits is provided with logic circuitry in a feedback loop for recording the presence of a desired input to the second plurality of latching circuits.

22. (Currently Amended) The ~~integrated~~ circuit of claim 21, wherein the desired input to the second plurality of latching circuits is a logic level high.

23. (Currently Amended) The ~~integrated~~ circuit of claim 1, further comprising a result calculator configured to provide information collected from the measure of jitter.

24. (Currently Amended) The ~~integrated~~ circuit of claim ~~23~~19, further comprising a~~wherein the~~ result calculator connected to the second plurality of latching circuits and~~is~~ configured ~~to provide~~ for receiving recorded pulses and based thereon providing information ~~of~~ on an earliest occurrence in the chain of the significant instant ~~on~~ of the propagating input clock signal.

25. (Currently Amended) The ~~integrated~~ circuit of claim ~~23~~19, further comprising a~~wherein the~~ result calculator connected to the second plurality of latching circuits and~~is~~ configured ~~to provide~~for receiving recorded pulses and based thereon providing information ~~of~~on ~~an~~ a latest occurrence in the chain of the significant instant ~~on~~ of the propagating input clock signal.

26. (Currently Amended) The ~~integrated~~ circuit of claim ~~23~~19, further comprising ~~a~~wherein ~~the~~ result calculator connected to the second plurality of latching circuits and~~is~~ configured ~~to provide~~for receiving recorded pulses and based thereon providing information ~~of~~ on a difference between an earliest and a latest occurrence in the chain of the significant instant ~~on~~ of the propagating input clock signal.

27. (Currently Amended) The ~~integrated~~ circuit of claim ~~23~~19, further comprising ~~a~~wherein ~~the~~ result calculator connected to the second plurality of latching circuits and~~is~~ configured ~~to provide~~for receiving recorded pulses and based thereon providing median or average information on the occurrences~~an average~~ of the significant instant ~~on~~ of the input clock signal.

28. Cancelled.

29. (Currently Amended) The ~~integrated~~ circuit of claim ~~23~~19, further comprising ~~a~~wherein ~~the~~ result calculator connected to the second plurality of latching circuits and~~is~~ configured ~~to provide~~for receiving recorded pulses and based thereon providing information on a standard deviation ~~of~~ in the occurrences of the significant instant ~~on~~ of the input clock signal.

30. (Currently Amended) The ~~integrated~~ circuit of claim 23, wherein the result calculator is configured to provide information responsive to a mode selection signal.

31. (Currently Amended) A method for measuring jitter of a ~~significant instant on a clock signal derived from a reference~~ clock signal, comprising:

for each of a plurality of trigger signal occurrences, performing the steps of

receiving ~~an input~~ the clock signal, ~~wherein~~ the ~~input~~ clock signal ~~has~~having a significant instant;

propagating the significant instant;~~delaying~~ of the ~~input~~ clock signal ~~by~~through a ~~first~~chain of delay elements, wherein each element has an associated delay and the chain has a total delay equal to ~~produce a delayed input clock signal and a~~

~~delayed significant instant on the delayed input clock signal~~the sum of the associated delays;

receiving a trigger signal~~, wherein~~ and delaying the received trigger signal ~~is delayed from the reference clock signal by~~to occur at a ~~second~~time equal to approximately ~~have~~half the total delay;~~detecting~~ of the ~~delayed significant instant on the delayed input clock signal; and~~chain;

detecting propagation of the significant instant of the clock signal through each of the delay elements in the chain and producing a pulse corresponding thereto;

recording any pulse that is coincident with the trigger signal; and

producing a jitter measurement signal responsive to the ~~delayed significant instant on the delayed input clock signal and the trigger signal.~~recorded pulses after the plurality of trigger signal occurrences.

32. (Currently Amended) The method of claim 31, further comprising deriving a jitter measure through a comparison of the jitter measurement signal to ~~the~~ an associated~~first~~ delay.

33. (Original) The method of claim 31, further comprising filtering the jitter measurement signal to produce a filtered jitter measurement signal.

34. (Currently Amended) The method of claim 33, wherein the filtered jitter measurement signal contains information of an earliest occurrence in the chain of the ~~delayed~~ propagating significant instant ~~on~~ of the ~~delayed~~ input clock signal.

35. (Currently Amended) The method of claim 33, wherein the filtered jitter measurement signal contains information of a latest occurrence in the chain of the ~~delayed~~ propagatingsignificant instant ~~on~~ of the ~~delayed~~ input clock signal.

36. Cancelled.

37. (Currently Amended) The method of claim 36, further comprising determining an earliest occurrence in the chain of the propagating significant instant.

38. (Currently Amended) The method of claim 36, further comprising determining a latest occurrence in the chain of the propagating significant instant ~~on the delayed input clock signal~~.

39. (Currently Amended) The method of claim 36, further comprising determining a difference between an earliest and latest occurrence in the chain of the propagating significant instant ~~on the delayed input clock signal~~.

40. (Currently Amended) The method of claim 36, further comprising determining ~~a~~ statistical information on the occurrences in the chain of the propagating significant instant ~~on the delayed input clock signal~~.

41. (Currently Amended) The method of claim 31, wherein an associated frequency of the reference clock signal is adjusted ~~responsive~~ in response to the jitter measurement signal.

42. (Currently Amended) The method of claim 31, wherein the ~~first~~ trigger delay is adjusted ~~responsive~~ in response to the jitter measurement signal.

43. (Currently Amended) The method of claim 31, further comprising receiving a reset signal, wherein the resent signal is delayed by a second delay relative to the reference clock signal which is adjusted ~~responsive~~ in accordance with~~to~~ the jitter measurement signal.

44. (Original) The method of claim 31, further comprising inputting the reference clock signal to a circuit to produce the input clock signal.

45. (Currently Amended) The method of claim 44, wherein the circuit is adjusted ~~responsive~~ in accordance with~~to~~ the jitter measurement signal.

46. (Currently Amended) A system for responding~~responsive~~ to jitter ~~in the system~~therein, comprising:

a reference clock configured to generate a reference clock signal having an associated

frequency;

a plurality of circuits configured to receive the reference clock signal and operative to generate an input clock signal, the plurality of circuits having a first set of characteristics; and

a jitter measurement sub-system configured to receive the reference clock signal and the input clock signal and operative to generate a jitter measurement output signal responsive to a significant instant of the input clock signal, wherein the jitter measurement sub-system includes:

a plurality of delay elements having a plurality of associated delays configured to generate a synthesized signal from the reference clock signal and the input clock signal; and

at least one programmable delay element having at least one associated programmable delay configured to produce a trigger signal for generating the jitter measurement output signal from the synthesized signal;

wherein the system is operative to adjust at least one parameter of the system ~~responsive~~ in accordance with~~to~~ the jitter measurement output signal.

47. (Original) The system of claim 46, wherein the at least one parameter of the system is at least one parameter of the jitter measurement sub-system.

48. (Original) The system of claim 46, wherein the at least one parameter includes the associated frequency.

49. (Original) The system of claim 46, wherein the reference clock signal further has an associated duty cycle, and the at least one parameter includes the associated duty cycle.

50. (Original) The system of claim 46, wherein the at least one parameter includes at least one characteristic from the first set of characteristics.

51. (Currently Amended) The system of claim 46, wherein the plurality of circuits includes a plurality of sub-circuits having a second set of characteristics, and wherein the at least one parameter includes at least one characteristic from the second set of characteristics.

52. (Currently Amended) The system of claim 46, wherein the output of one delay element is connected to the input of the next adjacent delay element~~each of the plurality of associated delays is equal~~.

53. (Currently Amended) The system of claim 46, wherein at least one of the plurality of associated delays is not equal to any other of the plurality of associated delays.

54. (Original) The system of claim 46, wherein the at least one parameter includes at least one of the plurality of associated delays.

55. (Original) The system of claim 46, wherein the at least one parameter includes all of the plurality of associated delays.

56. (Original) The system of claim 46, wherein the at least one parameter includes the at least one associated programmable delay.

57. (New) A jitter measurement circuit comprising:

a plurality of delay elements arranged in a series-connected chain having a total delay equal to the sum of the delays of the delay elements, wherein the first element in the chain has an input that receives an input clock signal, the chain propagating the input clock signal through each of its elements, and each delay element output producing a delayed version of the signal on its input;

a first set of circuitry operative to produce at an output a pulse corresponding to each delay element in response to the propagation of a significant instant of the input clock signal through the delay element, each pulse having a width that is approximately equal to the delay of the corresponding delay element; and

a second set of circuitry having one storage element corresponding to each output of the first set of circuitry, and an input that receives a trigger signal that is timed to correspond to a delay which is approximately half of the total delay of the chain, and the second set of circuitry being operative to record in the corresponding storage element any pulse that is active at the time of occurrence of the trigger signal, wherein a jitter measurement is made based on the pulses

recorded in the storage elements after a plurality of trigger signals has occurred.

58. (New) A circuit for jitter analysis as in claim 57, further comprising:

a single one detector for receiving a reset signal and for filtering the measure of jitter by selecting one instance of the recoded pulses in response to occurrence of the reset signal; and

a result calculator for producing statistical information about occurrences in the chain of the significant instance of the input clock signal.